IN THE CLAIMS

1-5. (Cancelled)

6. (Original) A multiple input/output magnetic random access memory device comprising:

a substrate having at least one block region, the at least one block region having a plurality of sub-block regions;

a plurality of digit lines extended in a first direction on the at least one block region, each of the digit lines being arranged along a second direction, the second direction being substantially perpendicular to the first direction;

a plurality of word lines arranged substantially parallel with the plurality of digit lines on the at least one block region;

a plurality of bit lines extended in the second direction on each of the sub-block regions, each of the bit lines being arranged along the first direction;

a plurality of magnetic memory cells disposed in intersections between the digit lines and the bit lines, the magnetic memory cells each including a rectangular free magnetic layer magnetized in a direction according to an externally applied magnetic field, a major axis of the rectangular free magnetic layer being substantially parallel to the first direction, and a minor axis of the rectangular free magnetic layer being substantially parallel to the second direction;

a row driver circuit that is configured to selectively activate the digit lines and the word lines, the row driver circuit being disposed at a first side of each of the block regions;

a first column driver circuit that is configured to selectively activate the bit lines for each of the sub-block regions, the first column driver circuit being disposed at a second side of each of the block regions;

a second column driver circuit that is configured to selectively activate the bit lines for each of the sub-block regions, the first column driver circuit being disposed at a third side of each of the block regions, the third side facing the second side;

a plurality of input/output lines; and

a sensing-and-writing driver circuit that is configured to selectively sense multiple bit lines for each of the sub-block regions to couple the sensed bit lines with the input/output lines, and configured to write data supplied from the input/output lines into corresponding multiple bit lines, the sensing-and-writing driver circuit being disposed between the second column driver circuit and the input/output lines.

7. (Original) The device of claim 6, the magnetic memory cell comprising:

a fixed magnetic layer having a fixed direction of magnetization, the fixed magnetic layer disposed over the digit lines;

an insulation layer disposed on the fixed magnetic layer; and

the rectangular free magnetic layer disposed on tunneling insulation layer and electrically coupled with the bit line.

8. (Original) The device of claim 6, the magnetic memory cell further comprising an antimagnetic layer facing a lower surface of the fixed magnetic layer.

9. (Original) The device of claim 6, the magnetic memory cell further comprising a switching element that is configured to be switched by each of the word lines to be electrically coupled with the fixed magnetic layer when the switching element is selected by the each of the word lines.

10-11. (Cancelled)